REMARKS

Applicants appreciate the Office Action of November 6, 2002. Applicants have amended the title of the invention as set out above to reflect the cancellation of the method claims responsive to a restriction requirement. Applicants respectfully submit that the pending claims are patentable over the cited references because the cited references fail to disclose or suggest many of the recitations of these claims. Accordingly, Applicants submit that the pending claims are in condition for allowance, which is respectfully requested in due course.

Amended Independent Claim 1 is Patentable Over Park

Claims 1-5 and 10-12 stand rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,774,327 to Park (hereinafter "Park"). Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited reference. For example, amended Claim 1 recites:

> An integrated circuit ferroelectric memory device, comprising:
> an integrated circuit transistor;
> a ferroelectric capacitor on the integrated circuit transistor having first and second sidewalls, the ferroelectric capacitor including a first electrode adjacent the transistor, a second electrode remote from the transistor and a ferroelectric film therebetween;
> **an insulating layer on the first and second sidewalls of the ferroelectric capacitor, the insulating layer having a surface that is substantially coplanar with an upper surface of the second electrode;** and
> a plate line directly on the ferroelectric capacitor.

Applicants submit that at least the highlighted portions of amended Claim 1 are neither disclosed nor suggested by Park.

Park recites:

> After forming the insulating layer 36, an insulating layer spacer 36a is formed as shown in FIG. 9. The insulating layer spacer 36a may be formed by performing an etching process so that the insulating layer 36 formed on the surface of the second electrode layer 34A opposite the high dielectric layer 33A is removed. **The surface of the high dielectric layer 33A opposite the first electrode layer 32A may be used as an ending point of the etching process.** Thus, as is seen in FIG. 9, even if a step difference B is generated at the edge of the second electrode layer 34A because of an overetch of the insulating layer to assure that all material is removed from the surface

> of the second electrode layer 34A, such a step difference B should not affect the electrical characteristics of the device.

See Park, column 6, lines 7-20. In other words, Park discusses using the high dielectric layer 33A (ferroelectric layer) as an etch stop layer. Using the high dielectric layer 33A as an etch stop layer may cause the high dielectric layer 33A to be exposed during an over etch of the insulating layer 36. This may cause deterioration of device characteristics. For example, exposing a sidewall of the high dielectric layer 33A may cause hydrogen damage during subsequent oxide deposition or annealing processes.

In contrast, amended Claim 1 recites "an insulating layer on the first and second sidewalls of the ferroelectric capacitor, **the insulating layer having a surface that is substantially coplanar with an upper surface of the second electrode**." In other words, the insulating layer is etched until the second electrode of the ferroelectric capacitor is exposed. Accordingly, even if the insulating layer were to be over etched, the ferroelectric film would not likely be damaged as discussed above with respect to Park. Anticipation under 35 U.S.C. § 102 requires the cited reference to teach every recitation of the claimed invention. Nothing in Park discloses or suggests an insulating layer that has a surface that is substantially coplanar with an upper surface of the second electrode. Accordingly, Park does not anticipate amended Claim 1.

For at least the foregoing reasons, Applicants respectfully submit that independent Claim 1 is patentable over Park. Applicants further submit that the dependent claims are patentable at least per the patentability of independent base Claim 1 from which they depend. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections with respect to Claims 1-5 and 10-12.

Amended Independent Claim 1 is Patentable Over Jung *et al.*

Claims 1-3, 5-7 and 10-12 stand rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,388,281 to Jung *et al.* (hereinafter "Jung"). Applicants respectfully submit that many of the recitations of amended Claim 1 are neither disclosed nor suggested by Jung. In particular, Applicants submit that at least the highlighted portions of Claim 1 set out above are neither disclosed nor suggested by Jung.

The Office Action points to Figure 2 of Jung as teaching the recitations of, for example, Claim 1 of the present invention. *See* Office Action, page 4. As illustrated in Figure 2 of Jung, the insulating layer 134 has a surface that is substantially higher than the surface of the second electrode 126,128 of Jung. In fact, the second electrode 126,128 is located in a contact hole defined by the sidewalls of the insulating layer 134. In contrast, Claim 1 recites an insulating layer on the first and second sidewalls of the ferroelectric capacitor, **the insulating layer having a surface that is substantially coplanar with an upper surface of the second electrode**. Nothing in Jung discloses or suggests an insulating layer having a surface that is substantially coplanar with an upper surface of the second electrode. As discussed above, anticipation requires the cited reference to teach every recitation of the claimed invention. Accordingly, Jung does not anticipate amended Claim 1.

For at least the foregoing reasons, Applicants respectfully submit that independent Claim 1 is patentable over Jung. Applicants further submit that dependent Claims 2-3, 5-7 and 10-12 are patentable at least per the patentability of independent base Claim 1 from which they depend. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections with respect to the pending Claims.

CONCLUSION

Applicants have shown that independent Claim 1 and the claims that depend therefrom are patentable over the cited references because the cited references fail to disclose or suggested all of the recitations of the claims. Accordingly, Applicants submit that the pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s), including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under

37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Respectfully submitted,

Elizabeth A. Stanek
Registration No. 48,568

Correspondence Address:

20792
PATENT TRADEMARK OFFICE
Telephone: 919/854-1400
Facsimile: 919/854-1401

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, DC 20231, on February 5, 2003.

Traci A. Brown
Date of Signature: February 5, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the title:

Please replace the title with the following new title:

--INTEGRATED CIRCUIT FERROELECTRIC MEMORY DEVICES INCLUDING PLATE LINES DIRECTLY ON FERROELECTRIC CAPACITORS [AND METHODS OF FABRICATING THE SAME]--

In the Claims:

1. (Amended) An integrated circuit ferroelectric memory device, comprising:

an integrated circuit transistor;

a ferroelectric capacitor on the integrated circuit transistor having first and second sidewalls, the ferroelectric capacitor including [having] a first electrode adjacent the transistor, a second electrode remote from the transistor and a ferroelectric film therebetween;

an insulating layer on the first and second sidewalls of the ferroelectric capacitor, the insulating layer having a surface that is substantially coplanar with an upper surface of the second electrode; and

a plate line directly on the ferroelectric capacitor.